

PATENT
DOCKET NO. A5GN2392US EXPRESS MAIL LABEL NO. EV229159482US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ken Gentile

Title: DIGITALLY-REALIZED SIGNAL GENERATORS AND METHODS

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT


Sir:

Enclosed is PTO Form 1449 (and a copy of the non-patent reference) for this application. The filing of this information disclosure statement shall not be construed as a representation that a search has been made (37 C.F.R. 1.97(g)), an admission that the information cited is, or is considered to be, material to patentability, or that no other material information exists.

The filing of this information disclosure statement shall not be construed as an admission against interest in any manner. Notice of January 9, 1992, 1135 O.G. 13-25, at 25.

Respectfully submitted,

December 11, 2003


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Form PTO-1449 INFORMATION DISCLOSURE CITATION IN AN APPLICATION <i>(Use several sheets if necessary)</i>										Docket Number (Optional) A5GN2392US					Application Number				
										Applicant Gentile, Ken									
										Filing Date					Group Art Unit				

U.S. PATENT DOCUMENTS														
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE								
	6 1 9 8 3 5 3	3/6/01	Janesch, et al.	331	16									
	6 3 2 6 8 5 1	12/4/01	Staszewski, et al.	331	17									
	6 4 0 4 2 4 7	6/11/02	Wang	327	158									
	6 4 2 9 9 0 1	8/6/02	Kiyose, et al.	348	500									
	6 4 7 3 4 7 8	10/29/02	Wallberg, et al.	375	376									
	6 5 4 2 0 3 9	4/1/03	Ogura	331	11									
	6 5 9 3 8 1 5	6/15/03	Takahashi	331	1A									

FOREIGN PATENT DOCUMENTS														
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION								
						YES	NO							

OTHER DOCUMENTS <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>														
		Dunning, Jim, et al., "An All-Digital Phase-Locked Loop with 50-Cycle Lock Time Suitable for High-Performance Microprocessors", IEEE Journal of Solid-State Circuits Vol 30, No. 4, April, 1995, pp. 412-422												

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP§609; Draw line through	